Amendments to the Specification:

Please replace the paragraph beginning on page 2, line 8 with the following amended paragraph:

As all the cells are transferred after the division, it is not necessary for a physical line to be occupied by one communication. Namely, it is desirable in the efficiency of using a line that ATM cells are transferred through the single line by being multiplexed. It looks like by the transmitting party that a dedicated line is provided for the cells to reach the opposite party by cell transmission through various lines. Such a line called virtual channel (VC). A number that is called virtual channel identifier [[(VC)]] (VCI) is designated to the virtual channel.

Please replace the paragraph beginning on page 3, line 6 with the following amended paragraph:

Referring to Fig. 1, a mobile telecommunication system comprises a [[bas]] base transceiver station 10, a base station controller 20 controlling the base transceiver station, a mobile switching center 30 constituting an interface point for a user traffic between switching centers.

Please replace the paragraph beginning on page 3, line 21 with the following amended paragraph:

Moreover, the ATM low rate subscriber multiplexing/demultiplexing board assembly 2 transmits an ATM cell to an ATM switch in the base station controller 20 and makes an SOC (start of cell) signal of the ATM cell become low active whenever transmitting a first byte of the ATM cell of 53 bytes, thereby storing the number in a dual port RAM (DPRAM) whenever the SOC signal becomes active. The location written in the dual port RAM is distinguished by indexing with VPI/VCI, which is read by a CPU of the ATM low rate subscriber multiplexing/demultiplexing board assembly 2 to ascertain how many cells [[□]] have passed through by the corresponding VPI/VCI.

Please replace the paragraph beginning on page 4, line 7 with the following amended paragraph:

In accordance with the number of storage in the dual port RAM, as mentioned in the above explanation, the number of the ATM cells inputted in the base station controller and the other number of the ATM cells outputted from the base station controller are monitored. Unfortunately, the ATM cell monitoring device according to the related art only monitors how many ATM cells are transmitted and received when transceiving an ATM cell consisting of 53 bytes yet fails to ~~monitors~~ monitor an error of the transceiving ATM cell and a delay time of the cell transmission from the base station controller to the base transceiver station.

Please replace the paragraph beginning on page 6, line 10 with the following amended paragraph:

A5

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the ~~inventing~~ invention and together with the description serve to explain the principle of the invention.

Please replace the paragraph beginning on page 6, line 19 with the following amended paragraph:

A6

Fig. 2 shows a block diagram of an asynchronous transfer mode cell monitoring device in a telecommunication system according [[t]] to the present invention.

Please replace the paragraph beginning on page 7, line 3 with the following amended paragraph:

A7

Fig. 2 shows a block diagram of an asynchronous transfer mode cell monitoring device in a telecommunication system according [[t]] to the present invention.

Please replace the paragraph beginning on page 7, line 6 with the following amended paragraph:

A8

Referring to Fig. 2, an ATM cell monitoring device 500 of a cell

multiplexing/demultiplexing device in a base station controller of a communication system includes an E1 matching part 300 consisting of a first to an nth E1 matcher 300a to 300n and enabling to perform E1 interface (2.048Mbps) by being connected to a base transceiver station 100, a multiplexing/demultiplexing part 200 (established in a base station controller) multiplexing and transmitting an ATM cell inputted from the E1 matching part 300 to an ATM switch 400 and then demultiplexing the ATM cell inputted from the ATM switch 400, a CPU 270 controlling the multiplexing/demultiplexing part 200, a GPS receiver 280 receiving a packet, an ATM switch 400 switching outputting ATM cells transceiving with the multiplexing/demultiplexing part 200.

Please replace the paragraph beginning on page 7, line 22 with the following amended paragraph:

The multiplexing/demultiplexing part 200 comprises a cell bus 291 through which ATM cells pass, a cell bus RX I/F 210 which multiplexes the ATM cells inputted from the first to nth matches 300a to 300n, adjusts the inputted ATM cells for the ATM cell requirements for the multiplexing/demultiplexing part 200 itself, carries out header error check (HEC) of the ATM cells, counts and records the number of error occurred in a first dual port RAM 240, a cell BUS TX I/F 220 transferring an ATM cell received from the ATM switch 400 or a test ATM cell to the E1 matching part 300 wherein the test ATM cell is generated from the CPU 270 for measurement of cell transmission time, a first dual port RAM 240 storing the number

of ATM cells inputted into the multiplexing/demultiplexing part 200 and the other number of the error-occurred ATM cells of the inputted ATM cells which are provided by the cell bus RX[[/]] I/F 210, a second dual port RAM 250 in which VPI index matched by each of the VPI/VCI is stored, a CAM (content addressable memory) 260 in which an address of the second dual port RAM 250 where the VPI index is stored, a first FIFO (first in first out) 230 storing temporarily the ATM cells received from the E1 matching part 300 wherein the ATM cells are to be read by the CPU 270, and a second FIFO (290) storing temporarily the test ATM cells generated from the CPU 270.

A9 Cont.

Please replace the paragraph beginning on page 9, line 14 with the following amended paragraph:

When the ATM cells to be monitored selectively exists by comparing the VPI/VCI of the ATM cells inputted to the cell bus RX[[/]]I/F [[270]] 210 to the other VPI/VCI latched with hardware, the CPU 270 directs the first FIFO 230 to store it when the cell bus RX[[/]] I/F 210 receives the ATM cells having the VPI/VCI field. In accordance with the direction, one the ATM cell to be monitored out of the whole ATM cells received by the base transceiver station 100 is received by the cell BUS RX I/F 210 and then recorded in the first FIFO 230, the CPU 270 checks the error occurrence through the entire cells by monitoring the recorded ATM cell of 53 bytes.

A10

Please replace the paragraph beginning on page 11, line 12 with the following amended paragraph:

Therefore, one the cell loop-backed from the base transceiver station 100 arrives in the cell multiplexing/demultiplexing part device and is stored in the first FIFO 230 by being received from the cell bus RX I/F 210, the CPU 270 enables to monitor the loop time (cell transmission delay time) by each VPI/VCI by comparing the transmission and receive [[time]] times with each other.